OPERATING AND SERVICE MANUAL

biomation

GOULD

Electronics & Electrical Products

Part Number 0112-0383 June 1981

MODEL K100-D LOGIC ANALYZER

ADDENDUM

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ADDENDUM

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5.3.2 RASTER SCAN DISPLAY ADJUSTMENT

Normally, the display should not require adjustment except as described in 5.3.1 of the K100-D Manual. Should further adjustment become necessary, the following additional adjustments are available on the Display Control Board.

1. Horizontal Oscillator Frequency, R2

Short the end of R25 or R26 nearest U3 to ground. Adjust R2 for the slowest possible horizontal roll. Remove the ground. Check that the display remains in sync when the unit is powered up, both when cold and after warm up.

2. Horizontal Phase, R10

Controls the start of the horizontal sweep relative to the video. If misadjusted, the characters on the left or right edge of the display may appear to be squeezed together or on top of each other.

3. Horizontal Linearity, L1

With the unit in timing mode and the trigger marker at 500, adjust for equal width on both sides of the trigger marker. L1 will interact with L2, horizontal width.

4. Vertical Linearity, R40

Adjust for equal character height at the top and bottom of the display.

5. Vertical Oscillator Frequency, R36

Short the end of R27 or R28 nearest U2 to ground. Adjust R36 for the slowest possible vertical roll. Remove the ground and insure that the display stops rolling.

6. Contrast, R24

Adjust together with the brightness control for the desired display. Normal adjustment is at or near maximum (full CW).

5.5.1 THRESHOLD CALIBRATION

The Threshold Calibration procedure in Section 5.5 assumes non-availability of the threshold summing test fixture. The procedures below are for those service centers having access to this fixture. Complete assembly instructions for the fixture can be found in Sections 5.8.1 and 5.8.2 of this addendum. Also included is the procedure for the latest revision to the threshold circuit for which the summing fixture must not be used.

Four different revisions of the K100-D Threshold/GPIB board have been manufactured. The calibration procedures differ somewhat from board to board. The different boards can be identified by the fabrication number etched on the solder side of the board as shown below:

I	0112-0042	ETCH A
II	0112-0042	ETCH B
III	0112-1042	ETCH A
IV	0112-1042	ETCH C and D

The summing test fixture consists of two 50 pin connectors of the type used for all probe and adapter inputs to the K100-D. The threshold voltage pins have been brought out to easily accessible test points. In addition, all 20 thresholds are tied to a common summing mode test point through 10kΩ, 1% resistors.

1. Calibration Using Summing Test Fixture

(For Type I and II Boards)

Install the summing test fixture in the probe sockets on the front panel of the K100-D. Turn the unit ON and allow 2 to 3 minutes for the power supplies to stabilize.

Proceed with the calibration procedure as in Section 5.5 of the manual using the test point labeled "N" on the fixture for all voltage adjustments instead of IC 1E pin 1. Use the labeled test points on the fixture instead of the IC pins to check the individual channel tolerances.

If the individual channels are not within the specified limits on Type I or II Boards, proceed with the channel gain calibration.

2. Channel Gain Calibration (Type I and II Boards Only)

Select threshold "VAR A" for all channels. SPECIFY "VAR A" -6.40V and depress Auto Arm.

Monitor the Channel A (Type I Boards) or Channel 0 (Type II Boards) test point on the summing test fixture. Adjust "A0" for +6.40V at the test point.

Monitor each of the remaining channel test points, and adjust the channel gain pot for each channel for +6.40V. (See Figures 5.11 and 5.12 for adjustment locations).

Return the DVM to the Channel A (Type I) or Channel 0 (Type II) test point. SPECIFY "VAR A" +6.35V and depress AUTO ARM. Adjust "AG" (see Figure 5.11) for a reading of -6.35V. Monitor each of the remaining channel test points, and adjust the appropriate channel gain pot for a reading halfway between the initial reading and -6.35V.

EXAMPLE: Before adjustment, the DVM reads -6.30V.
Adjust the channel gain pot for a reading of -6.325V.

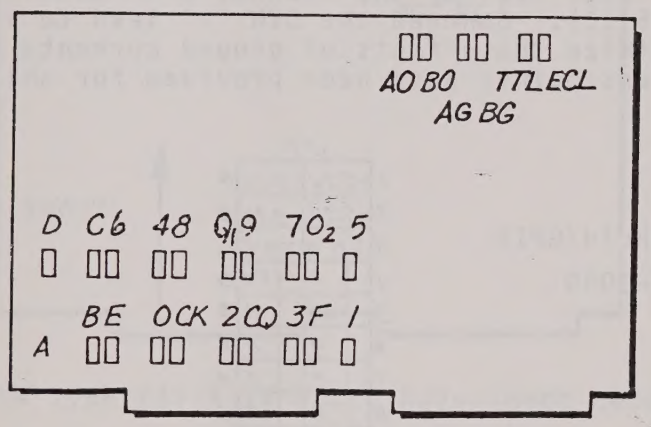


Figure 5.11 Type I Threshold Board Adjustment Locations

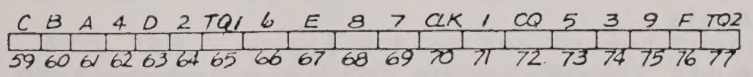


Figure 5.12 Type II Threshold Board Adjustment Locations

After completing the channel gain adjustments, repeat Section 1.

3. Threshold Calibration (Type III and IV Boards Only)

Place the Threshold/GPIB Board on the extender. Turn the unit ON and allow 2 to 3 minutes for the power supplies to stabilize.

Insure that either the standard probe set or the K100-D/10 Probe Pods are connected to both 50 pin connectors on the front panel. This is necessary because the output stages of Type IV Boards are load sensitive. The probes present a load of approximately 20kΩ to the threshold circuit.

Using a DVM, monitor the Channel 0 threshold at pin L of J7/P7 (see Figure 5.13). Connect the DVM "-" lead to a ground on the board to minimize the effects of ground currents on the voltage readings. Test points have been provided for this purpose.

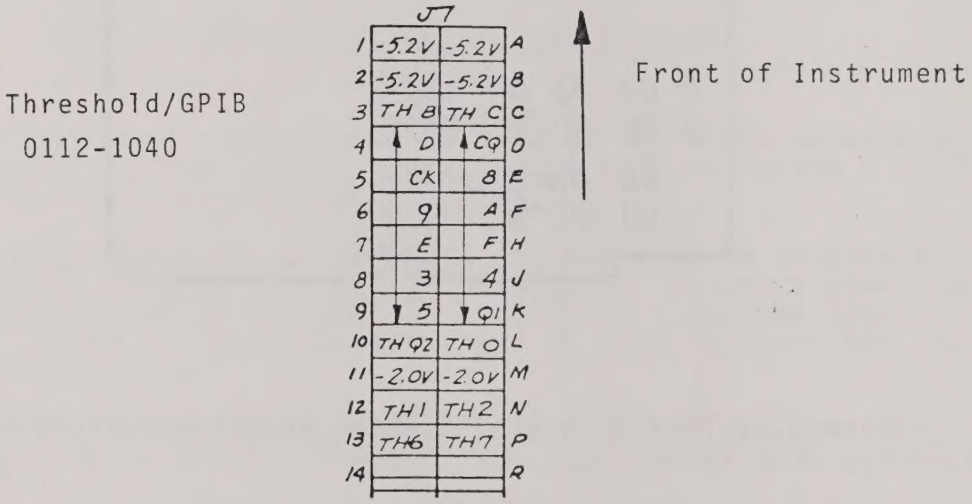


Figure 5.13-Threshold Board Edge Connector Labels

Select all thresholds to ECL and depress AUTO ARM. Adjust "E" for +1.30V at the Channel 0 test point. Verify +1.30V ±25mV on all channels.

Select all thresholds to "TTL" and depress AUTO ARM. Adjust "T" for -1.40V at the Channel 0 test point. Verify -1.40V ±25mV at the channel 0 test point. Verify -1.40V ±25mV on all channels.

Select all thresholds to "VAR A".

SPECIFY "VAR A" -6.40V and depress AUTO ARM. Adjust "AG" for +6.40V at the Channel 0 test point. Verify +6.40V ±25mV on all channels.

SPECIFY "VAR A" 0.00 and depress AUTO ARM. Adjust "A0" for 0.00 at the channel 0 test point. Verify 0.00 ±25mV on all channels.

SPECIFY "VAR" +6.35V and depress AUTO ARM. Check for -6.35V ±25mV on all channels.

Repeat the variable threshold alignment using "VAR B." "BO" and "BG" respectively instead of "VAR A", "AO" and "AG".

No further adjustment to Type III and IV Boards is possible. Failure to meet specification indicates a circuit malfunction.

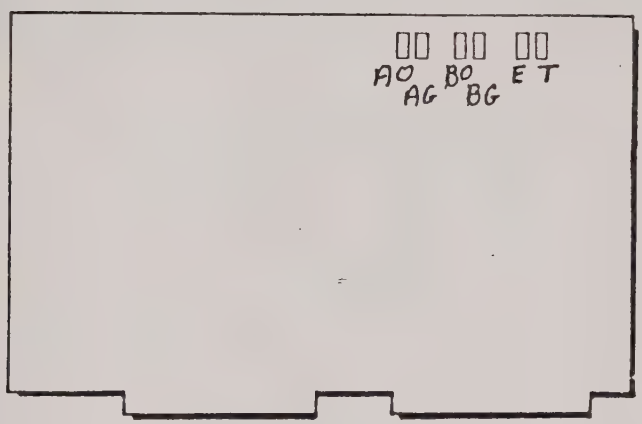


Figure 5.14 Type III & IV Board Adjustment Locations

5.7.1 Clock Calibration

Place the Record Control Board on the extender. Turn the unit ON. Select the clock source to INT 10ns.

Connect the oscilloscope to the junction of R5 and R6 (located in the upper left hand corner of the board). Connect the scope ground to the top end of R6. Use the shortest possible ground wire. Refer to Figure 7.8 in the manual for test point and adjustment locations.

Depress AUTO ARM. Adjust R48 on the Record Control Board for a waveform that is symetrical around the ECL threshold of -1.3V.

Remove the scope and connect a counter having a high input impedance to the same test point. Adjust C46 for a frequency of 100MHz ± 50kHz (0.05%).

NOTE: Early production units did not have C46 installed. To adjust the clock frequency on these units, it is necessary to select the values of C10 and C11. The nominal values were 47pF for C10 and 30pF for C11.

Turn the K100-D off and then on again. Insure that the oscillator frequency is unchanged.

If the oscillator has jumped to a higher frequency (1-3 MHz high), readjust C46 for a slightly lower frequency and repeat this test.

Turn the unit off and reinstall the Record Control Board in the chassis position.

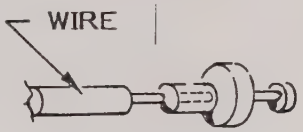
5.8.1 Threshold Alignment Fixture Input A

On connector housing 6000-0262 perform the following:

1. Drill size #44 3/32" 11 places and label as shown in **Figure 5.16**. Notch as shown in **Figure 5.15**

2. Wire terminals as follows:

   11 PLC
   TURRET TERMINAL
   (6200-0005)



QUANTITY	SOLDER ON LENGTH	LOCATION
2	3/4"	N,F
4	1"	B,C,D,E
2	1½"	8,A
1	1¼"	9
2	2"	CK, CQ

½ REAR VIEW

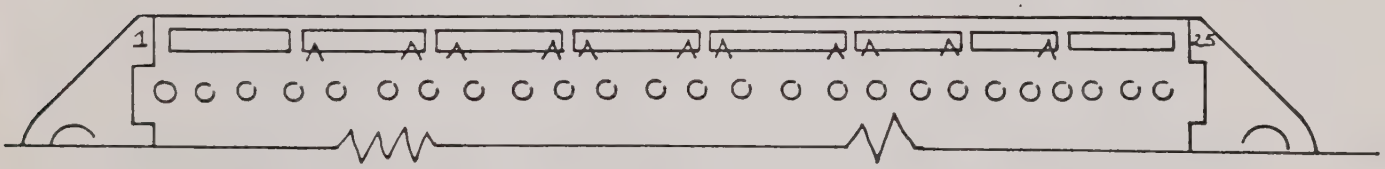


Figure 5.15- Rear View of Alignment Housing A

TOP VIEW

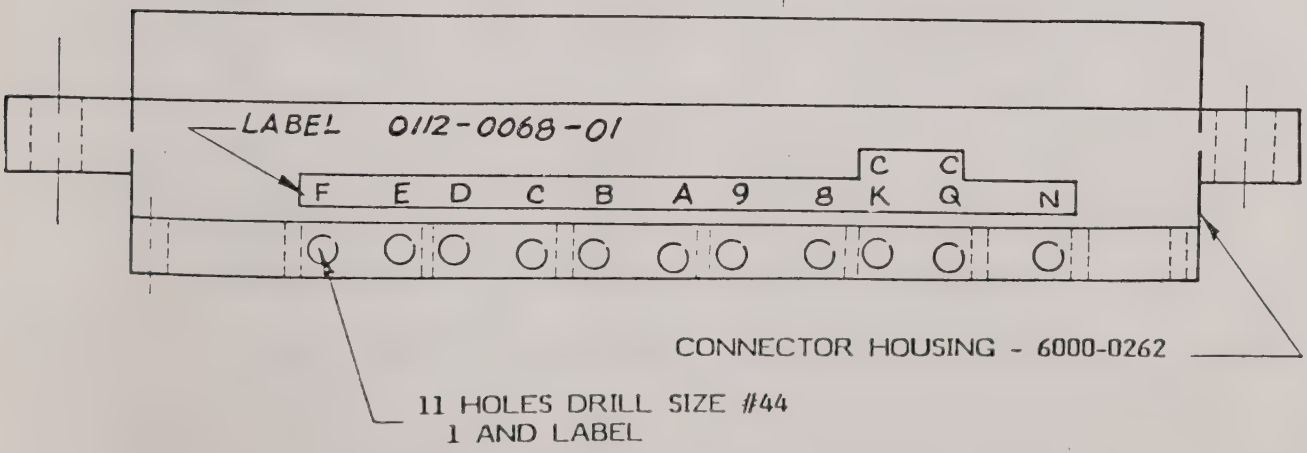


Figure 5.16- Top View of Alignment Housing A

3. Install terminals with krazy glue as shown in **Figure 5.17** and wire as you go, as shown in **Figure 5.18**

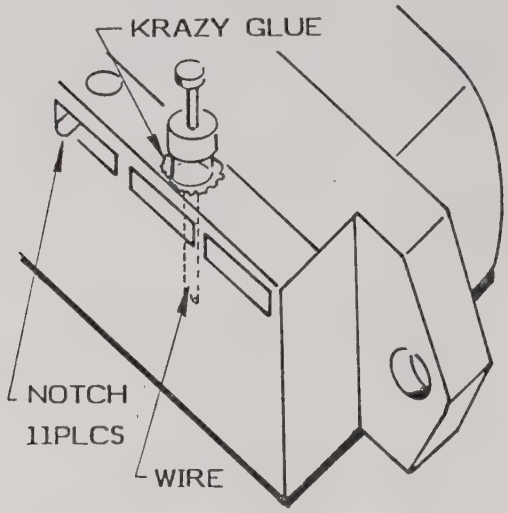


Figure 5.17-Alignment Fixture 'A' Terminal Post

WIRE ROUTING FROM TERMINAL	TO PIN	FROM	TO PIN
CQ	30 - 2"	B	18 - 1"
CK	3 - 2"	C	40 - 1"
8	50 - 1½"	D	13 - 1"
9	23 - 1¼"	E	35 - 1"
A	45 - 1½"	F	8 - 3/4"
		N	COM - 3/4"

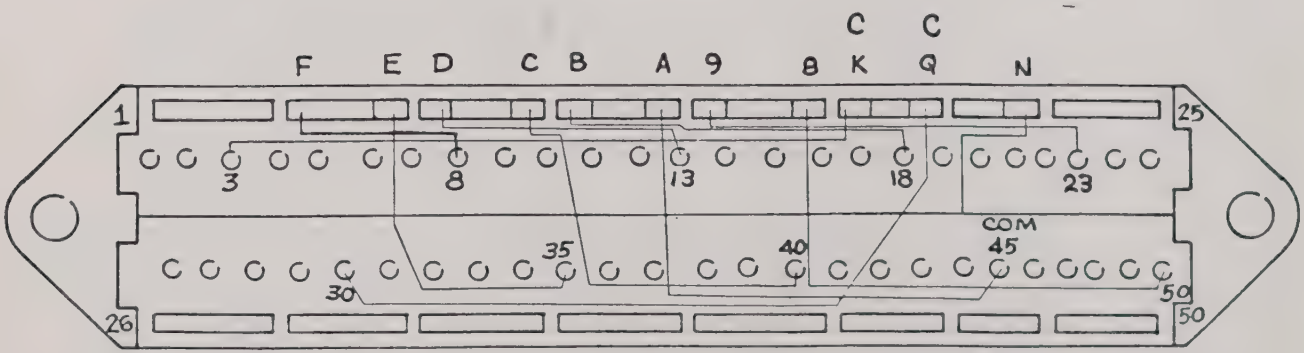


Figure 5.18-Alignment Fixture 'A' Wiring Diagram

NOTE: Follow wire routes as shown in **Figure 5.18**

4. Solder resistors to common bus wire as shown in **Figure 5.20**

5. Case up.

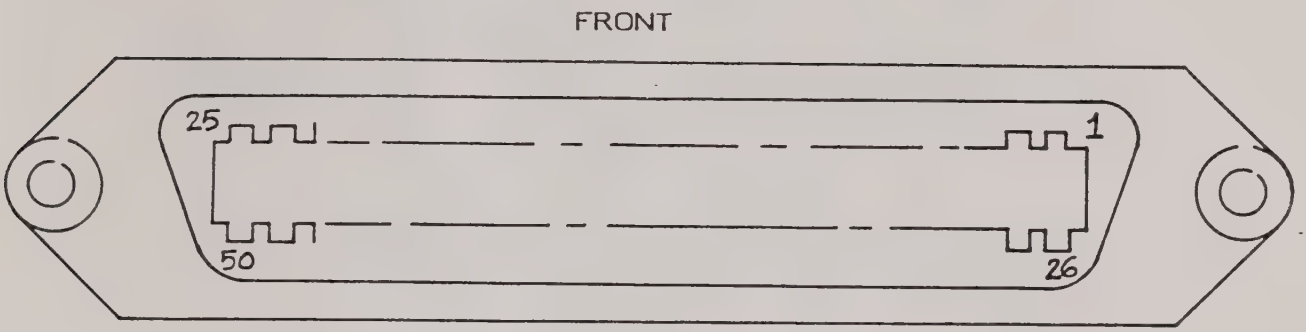


Figure 5.19-Front View of Alignment Housing A

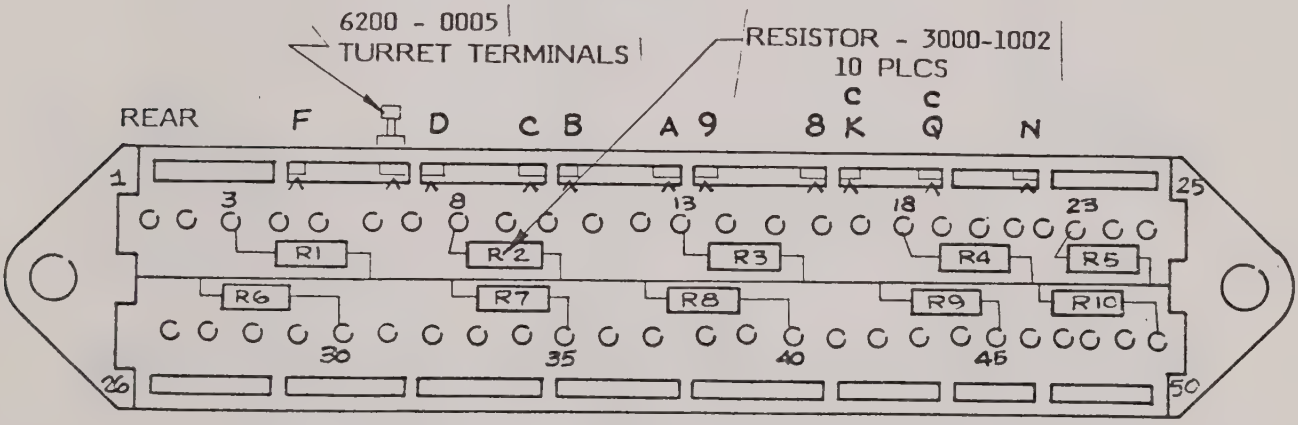


Figure 5.20-Alignment **Housing** A Resistor Placement

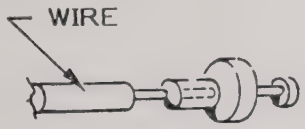
Resistor	From Pin #	To Bus Wire
R_1	3	Common
R_2	8	
R_3	13	
R_4	18	
R_5	23	
R_6	30	
R_7	35	
R_8	40	
R_9	45	Common

5.8.2 Threshold Alignment Fixture Input B

1. Drill size #44 3/32" 12 places and label as shown in **Figure 5.22** Notch as shown in **Figure 5.21**

2. Wire terminals as follows:

12 PLCS
TORRET TERMINALS
(6200-0005)



LOCATION	QUANTITY	SOLDER ON LENGTH
GND,7	2	$\frac{1}{4}$"
5	1	3/4"
N,3	2	1"
6,1	2	$1\frac{1}{4}$"
0	1	$2\frac{1}{2}$"
4	1	3
2,Q2	2	$5\frac{1}{2}$"
Q1	1	7"

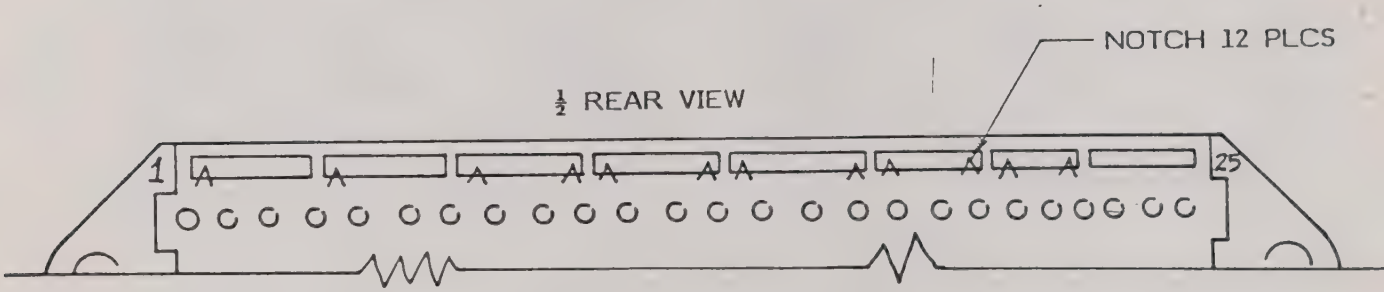


Figure 5.21-Rear View of Alignment Housing B

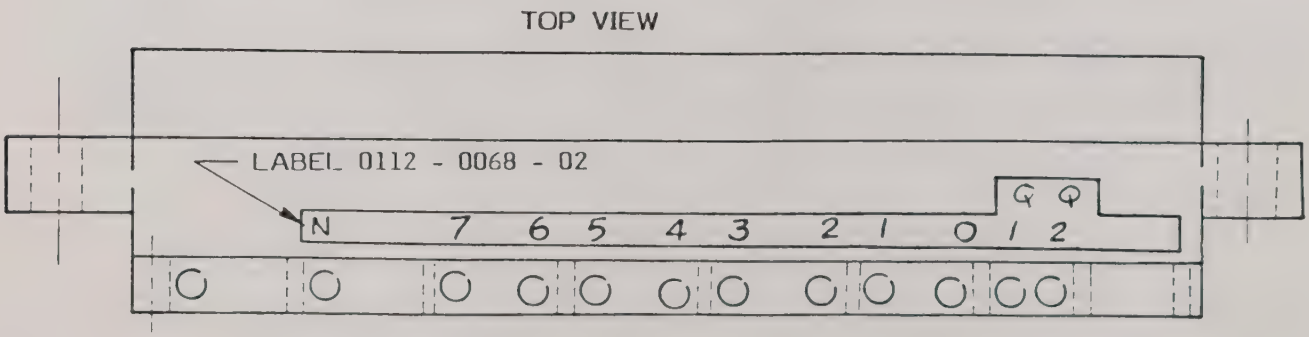


Figure 5.22-Top View of Alignment Housing B

3. Install terminals with krazy glue, as shown in **Figure 5.23** and wire as you go, as shown in **Figure 5.24**

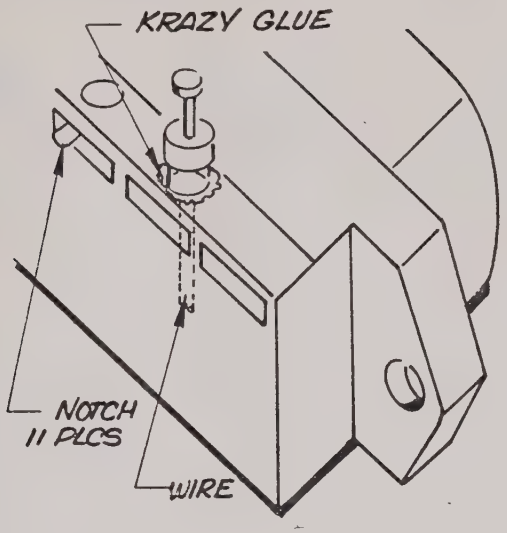


Figure 5.23-Alignment Fixture 'B' Terminal Post

WIRE ROUTING FROM TERMINAL	TO PIN	LENGTH OF WIRE	FROM TERMINAL	TO PIN	LENGTH OF WIRE
Ground	1	$\frac{1}{4}$"	3	18	1"
N	Common	1"	2	45	$5\frac{1}{2}$"
7	8	$\frac{1}{4}$"	1	23	$1\frac{1}{4}$"
6	35	$1\frac{1}{4}$"	0	50	$2\frac{1}{2}$"
5	13	3/4"	Q1	30	7"
4	40	3"	Q2	3	$5\frac{1}{2}$"

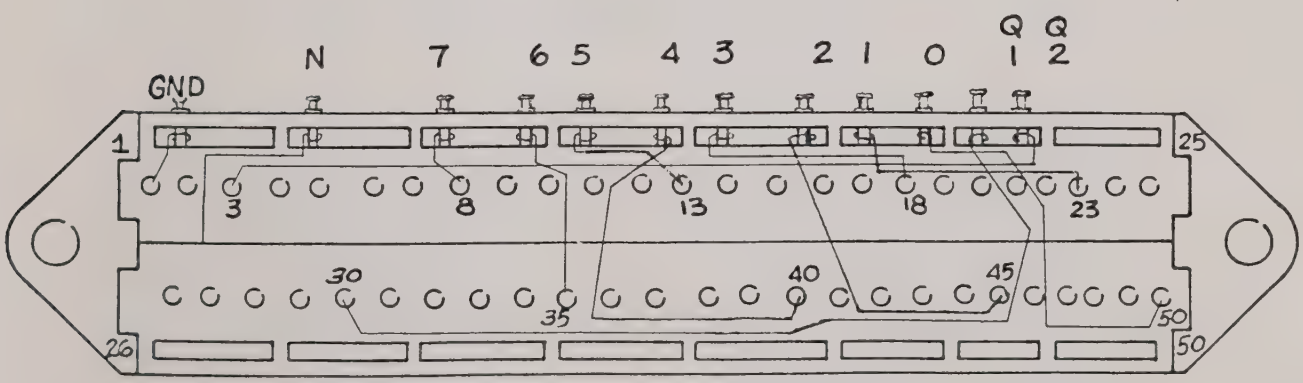


Figure 5.24-Alignment Fixture 'B' Wiring Diagram

4. Solder resistors to common bus wire as shown in **Figure 5.26**

5. Case up.

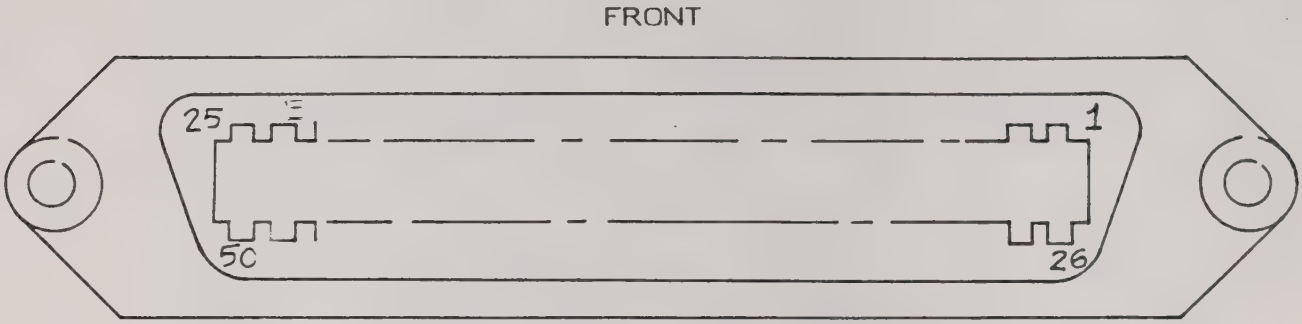


Figure 5.25-Front View of Alignment Housing B

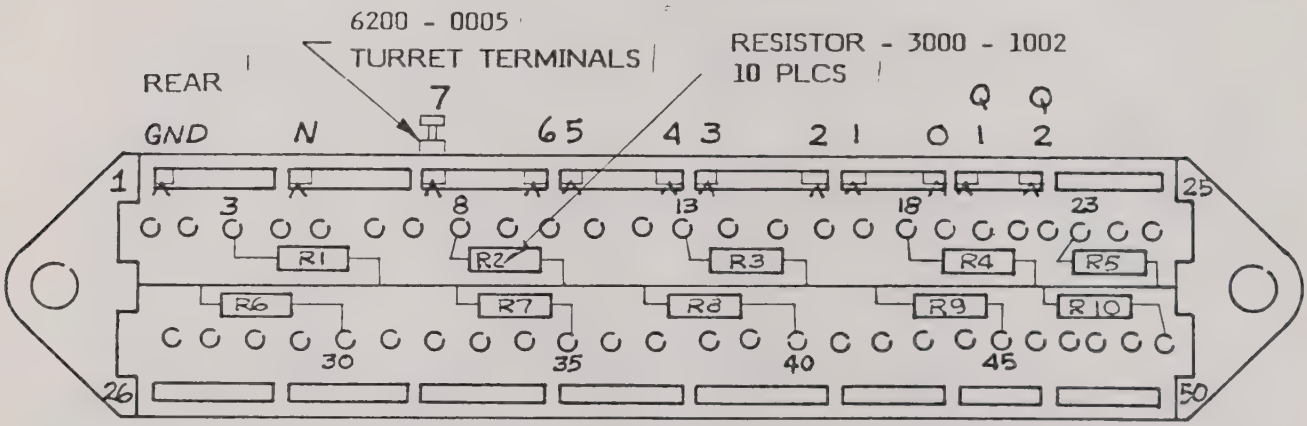


Figure 5.26-Alignment Housing B Resistor Placement

Resistor	From Pin #	To Bus Wire
R_1	3	Common
R_2	8	
R_3	13	
R_4	18	
R_5	23	
R_6	30	
R_7	35	
R_8	40	
R_9	45	Common

(Note: Affects Serial #28264 and on)

5.6.1 RECORD MEMORY ADJUSTMENTS

Remove the "0-F" memory board (see Figure A) and put on an extender. Turn the power on. Tests are performed using power up status mode.

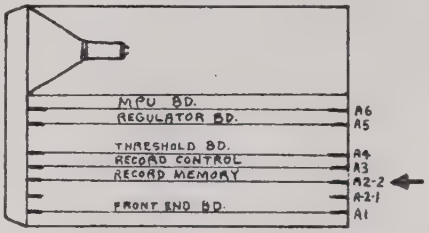


Figure A- Top View of K100-D Logic Analyzer

NOTE: Suggest using a Tek 485 or comparable oscilloscope for the following adjustments.

1. If there is an error in power up, Keystroke CE.

2. Keystroke TRIGGER xxxx xxxx xxxx xxxx. This assures a clean signal for calibration.

3. Keystroke AUTO ARM. The status byte in the lower left corner of the screen should indicate (TG?).

4. Monitor test point IC 1F pin 20 (WE) with Channel A of scope. With Channel B monitor test point IC 1F pin 3 (ADDR 1). GND on pin 19. Synchronize scope to Channel A.

NOTE: Superimpose the two patterns so as to create a common TTL threshold (+1.4 VDC).

Adjust D1 (R46) for 10ns between the last address edge and falling edge of the WE pulse. (Fig. B)

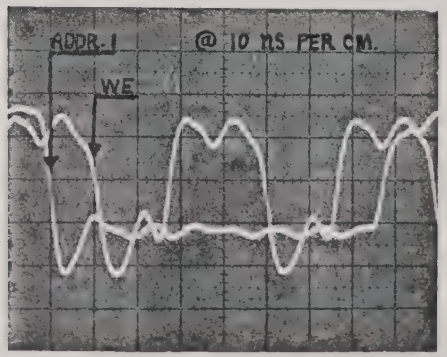


Figure B-Scope Display

Adjust W1 (R50) for 10ns between the WE rising edge and the first address edge (Fig. C)

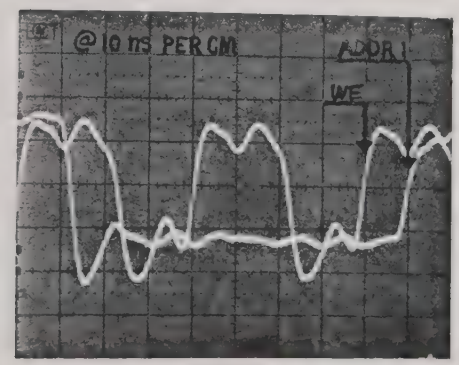


Figure C-Scope Display

5. Repeat the procedure for Ø2, Ø3, and Ø4. (See figure D and Table 1.0)

6. Turn the power off and return the Record Memory Board to its chassis position.

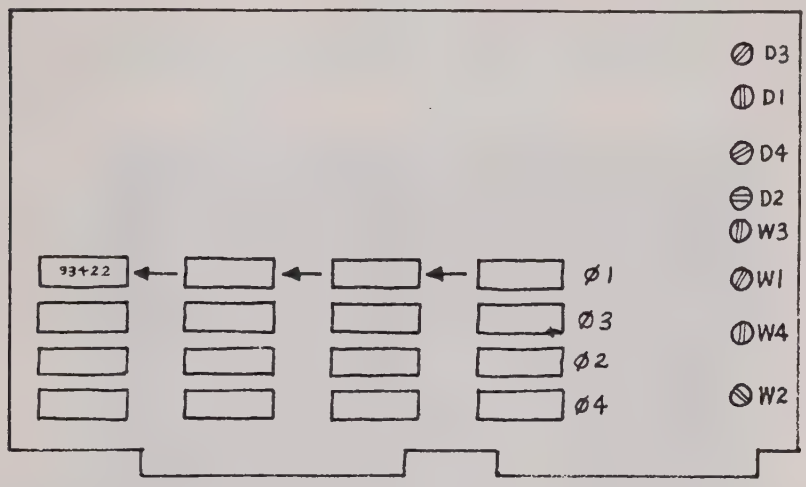


Figure D-Record Memory Board Calibration Layout

Table 1.0-Testpoint and Adjustment Locations

TESTPOINT		ADJUST
Ø1	1F20	W1(R50)
	1F3	D1(R46)
Ø2	1J20	W2(R52)
	1J3	D2(R48)
Ø3	1H20	W3(R49)
	1H3	D3(R45)
Ø4	1K20	W4(R51)
	1K3	D4(R47)

This information is applicable
only to serial #28264 and on

6.2.2 Memory Failure Chart

The following setup shows how to read the failure chart when working with the new Memory Board (0112-1020). Refer to Fig. A. (page 168)

HIGH SPEED RECORD MEMORY ERRORS

ADDRESS/PHASE	FEDC	BA98	7654	3210 (Channel Designation)
3/3	ØØØØ	1111	11ØØ	ØØØØ written (To Memory)
	ØØØØ	1111	Ø111	ØØØØ read (From Memory)

(Phase of Sample Clock Failed)

(Location Addressed in Memory)

Notice upon reading this chart that Channel Designation 7654 has 11ØØ written and Ø111 read out of memory. This shows incorrect data at Memory Address 3, Sample Clock Phase Ø3.

PHASE LOCATION ON PCB

Phase Ø1	Row F
Phase Ø2	Row J
Phase Ø3	Row H
Phase Ø4	Row K

CHANNEL LOCATION ON PCB

Channel	Column
0,1,2,3	1
4,5,6,7	3
8,9,A,B	5
C,D,E,F	7

Locate the channel where the failure to read back what was written in occured. Determine the phase of failure and its location in memory. Verify the inputs on the failed memory I.C. See Table 1.

Table 1-Memory Failure Location Chart

Channel	0,1,2,3	4,5,6,7	8,9,A,B	C,D,E,F
Phase				
1	1F	3F	5F	7F
3	1H	3H	5H	7H
2	1J	3J	5J	7J
4	1K	3K	5K	7K

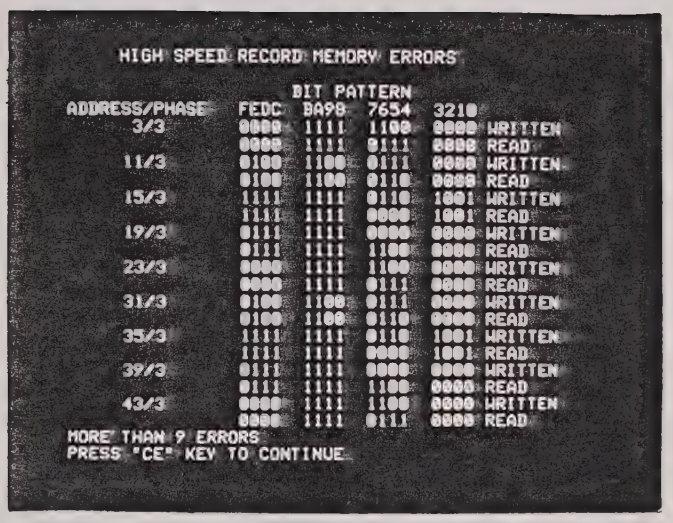
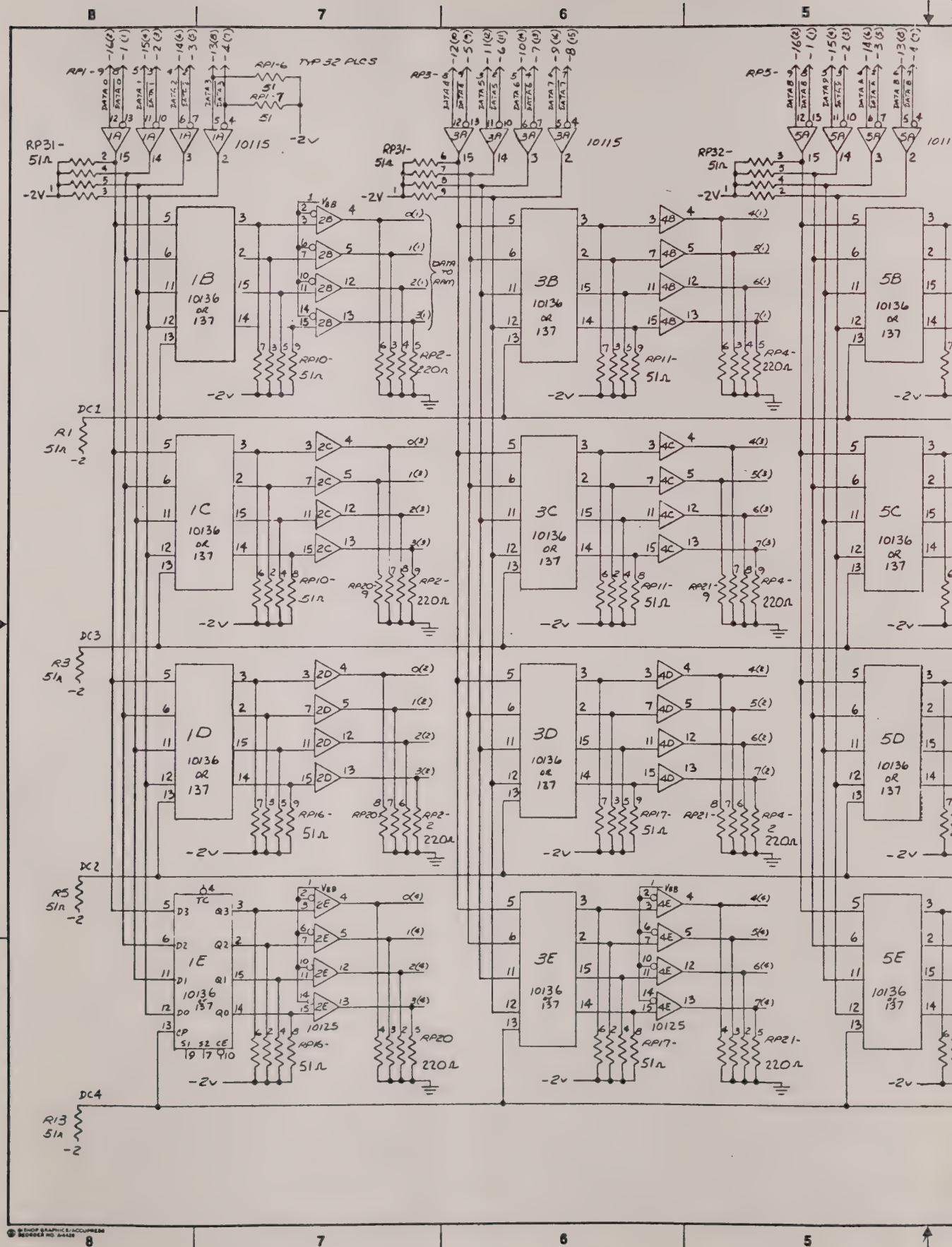
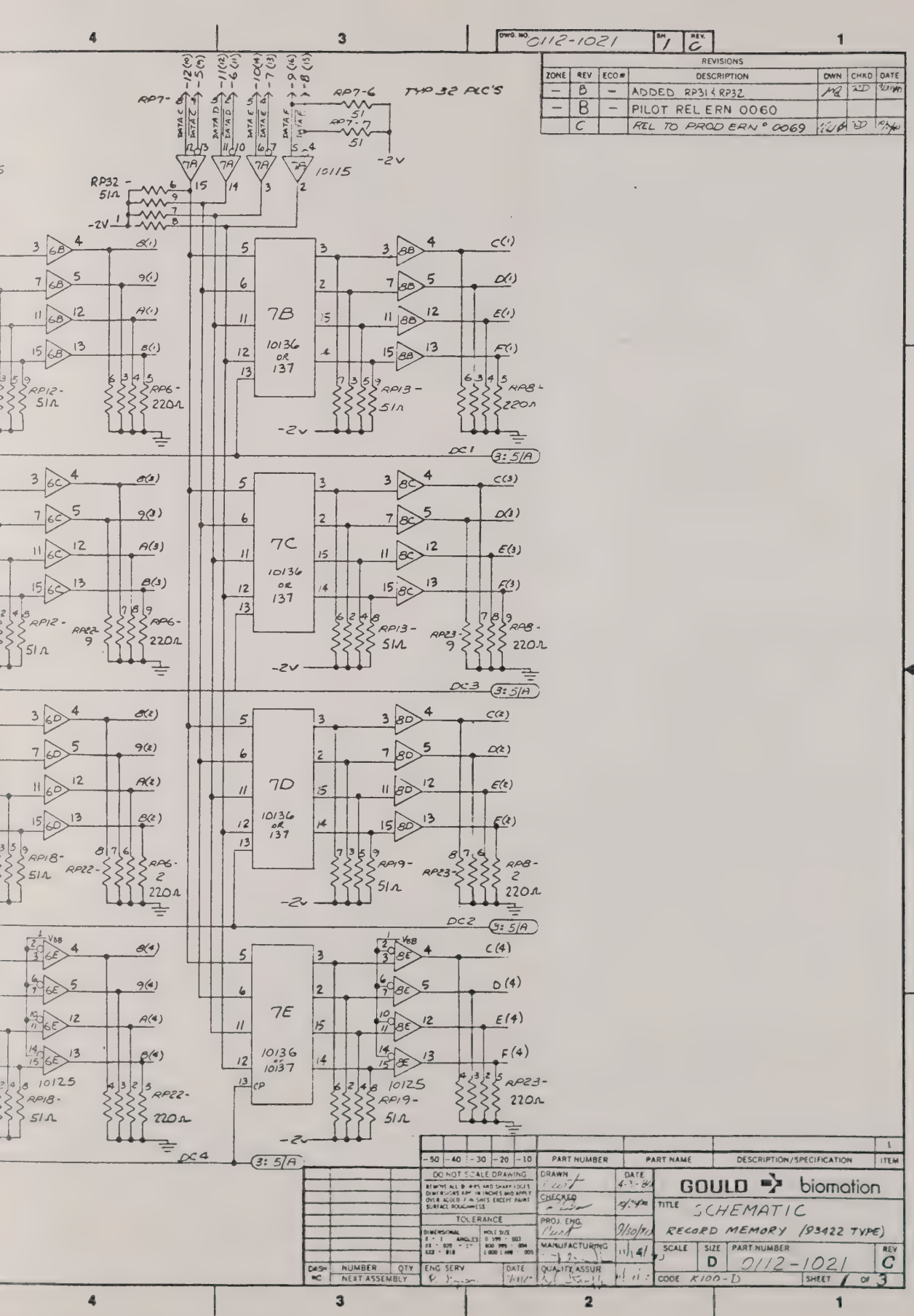
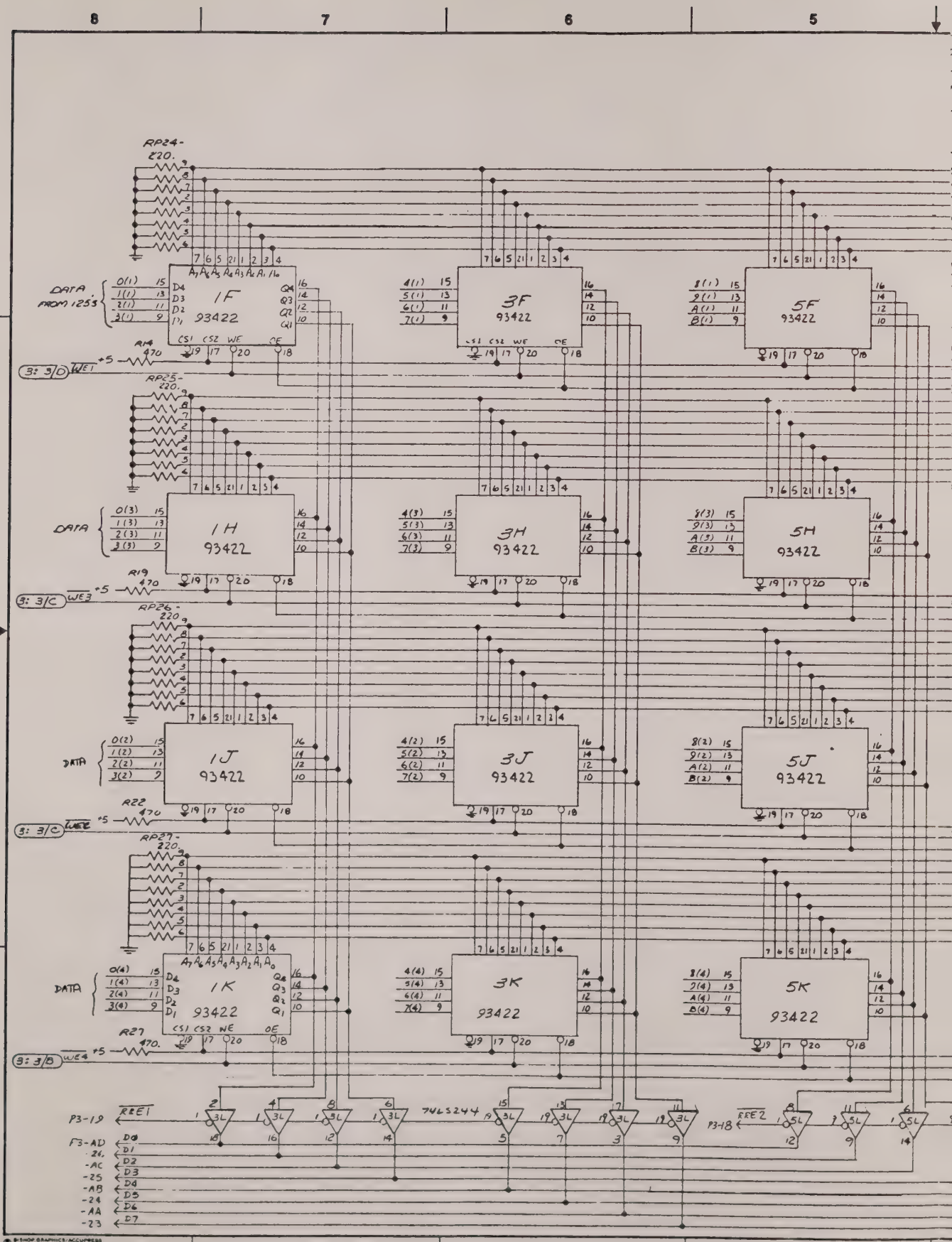


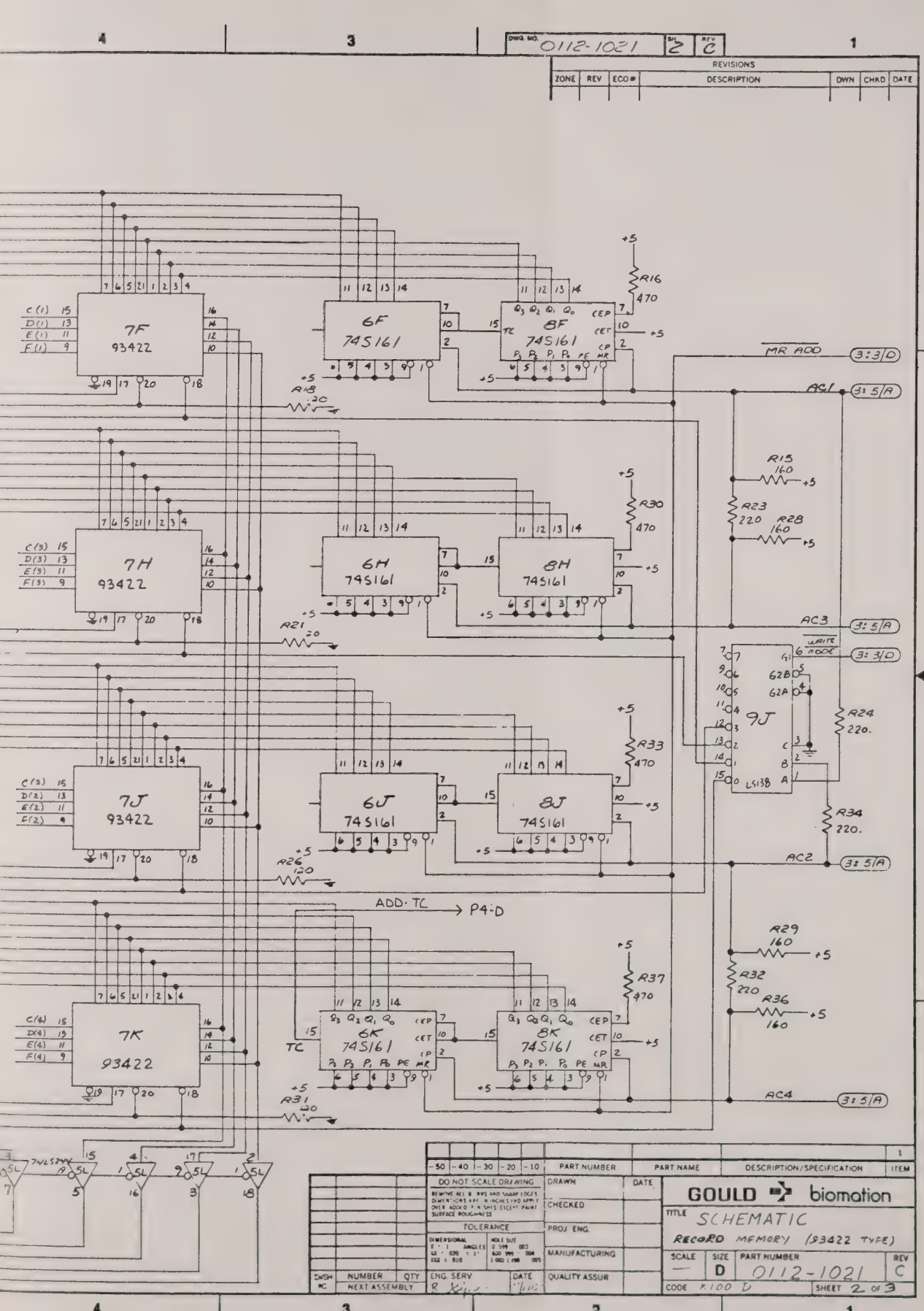
Figure A-High Speed Error Indication

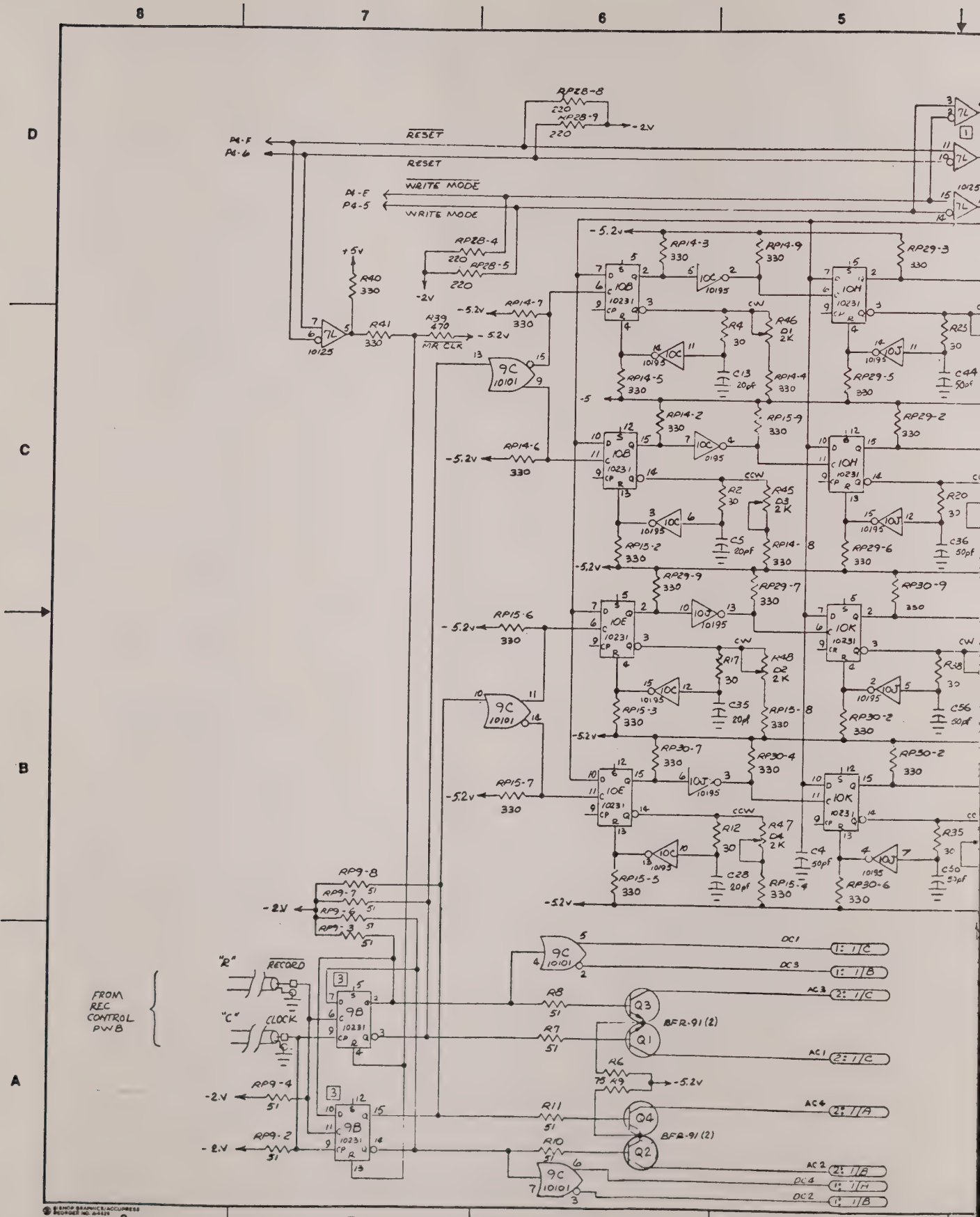
The ERROR light starts to blink 6 to 13 seconds after power on. A display similar to the above appears on the CRT.


B
7
6
5
D
C
B
A
RP1-9
RP1-6 TYP 32 PLCS
RP1-7
51
-2V
RP31-
51Ω
10115
RP3-
RP5-
RP32-
1B
10136 OR 137
3B
5B
1C
3C
5C
1D
3D
5D
1E
3E
5E
DATA TO RAM
RP10-
RP11-
RP2-
RP4-
220Ω
DC1
DC2
DC3
DC4
R1
R3
R5
R13
10125

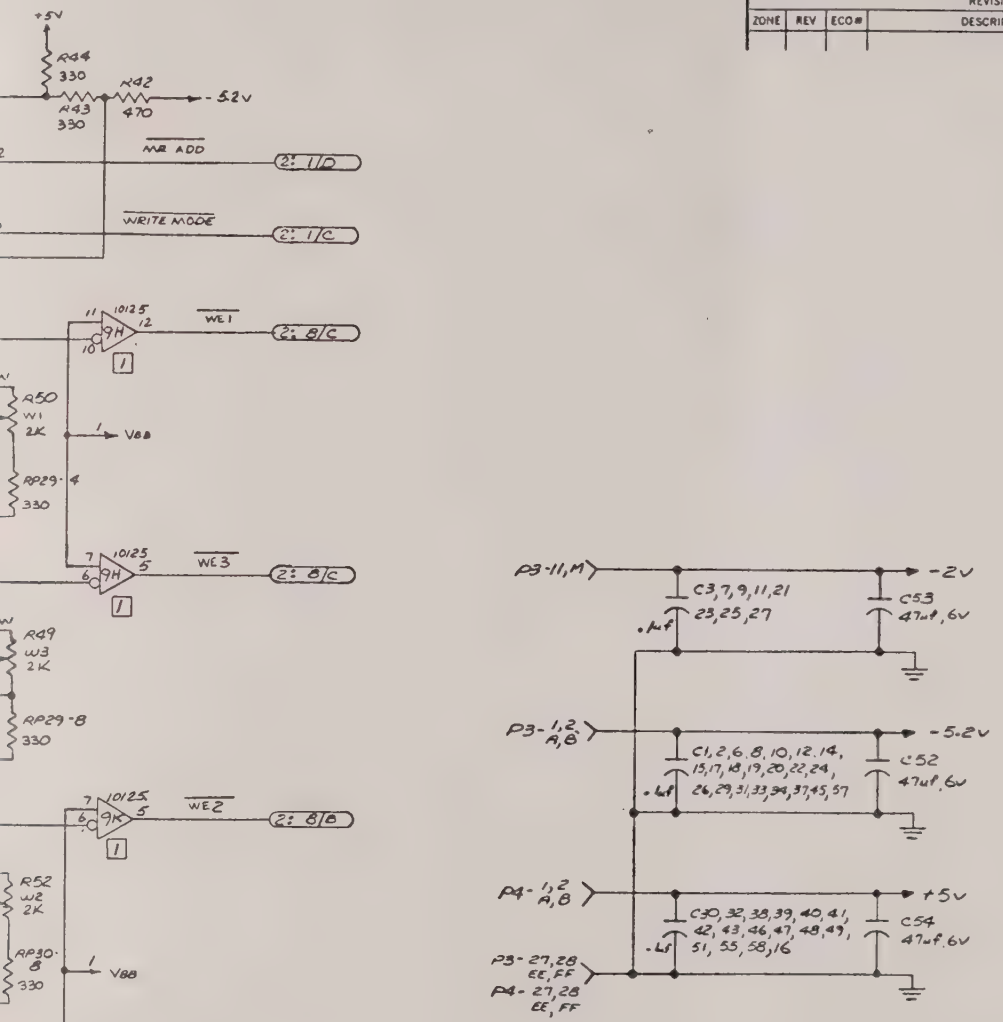

DWG. NO. 0112-1021
SH 1
REV C
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
— | B | — | ADDED RP31 & RP32
— | B | — | PILOT REL ERN 0060
| C | | REL TO PROD ERN # 0069
RP7-6
RP7-7
51
-2V
TYP 32 PLC'S
10115
RP32 - 51Ω
7A
7B
7C
7D
7E
10136 OR 137
10136 OR 137
10125
10125
RP6- 220Ω
RP8- 220Ω
RP12- 51Ω
RP13- 51Ω
RP18- 51Ω
RP19- 51Ω
RP22- 220Ω
RP23- 220Ω
DC1
DC3
DC2
DC4
3: 5/A
PART NUMBER
PART NAME
DESCRIPTION/SPECIFICATION
ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ. ENG.
MANUFACTURING
ENG SERV
QUALITY ASSUR
DATE
GOULD biomation
TITLE SCHEMATIC
RECORD MEMORY (93422 TYPE)
SCALE D
SIZE
PART NUMBER 0112-1021
REV C
CODE K100-D
SHEET 1 OF 3
DASH NO.
NUMBER
QTY
NEXT ASSEMBLY


8
7
6
5
D
C
B
A
RP24-
220.
DATA
FROM 1253
0(1)
1(1)
2(1)
3(1)
1F
93422
3F
4(1)
5(1)
6(1)
7(1)
5F
8(1)
9(1)
A(1)
B(1)
CS1 CS2 WE OE
R14
470
+5
3: 3/D
WE1
RP25-
220.
1H
0(3)
1(3)
2(3)
3(3)
3H
4(3)
5(3)
6(3)
7(3)
5H
8(3)
9(3)
A(3)
B(3)
R19
3: 3/C
WE3
RP26-
1J
0(2)
1(2)
2(2)
3(2)
3J
4(2)
5(2)
6(2)
7(2)
5J
8(2)
9(2)
A(2)
B(2)
R22
WE2
RP27-
1K
0(4)
1(4)
2(4)
3(4)
3K
4(4)
5(4)
6(4)
7(4)
5K
8(4)
9(4)
A(4)
B(4)
R27
470.
3: 3/B
WE4
P3-19
RRE1
74LS244
P3-18
RRE2
F3-AD
-24
-AC
-25
-AB
-24
-AA
-23
D0
D1
D2
D3
D4
D5
D6
D7


DWG NO. 0112-1021
SHT 2
REV C
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
7F 93422
6F 74S161
8F 74S161
7H 93422
6H 74S161
8H 74S161
7J 93422
6J 74S161
8J 74S161
7K 93422
6K 74S161
8K 74S161
9J LS138
R16 470
R30 470
R33 470
R37 470
R18 220
R21 220
R26 220
R31 220
R15 160
R23 220
R28 160
R24 220.
R34 220.
R29 160
R32 220
R36 160
MR ADD
ASI
AC3
AC2
AC4
WRITE MODE
ADD·TC → P4:D
TC
3:3/D
3:5/A
3:3/D
3:5/A
3:5/A
3:5/A
74LS27 MK
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV
DATE
GOULD biomation
TITLE SCHEMATIC
RECORD MEMORY (93422 TYPE)
SCALE —
SIZE D
PART NUMBER 0112-1021
REV C
CODE K100 D
SHEET 2 OF 3


RESET
WRITE MODE
RP28-8
220
RP28-9
220
-2V
RP28-4
220
RP28-5
220
+5V
R40
330
R41
330
R39
470
MR CLR
-5.2V
RP14-3
330
RP14-9
330
RP14-7
330
RP14-5
330
RP14-4
330
RP14-6
330
RP14-2
330
RP15-9
330
RP15-2
330
RP15-6
330
RP29-9
330
RP29-7
330
RP15-3
330
RP15-8
330
RP15-7
330
RP30-7
330
RP30-4
330
RP15-5
330
RP15-4
330
RP29-3
330
RP29-5
330
RP29-2
330
RP29-6
330
RP30-9
330
RP30-2
330
RP30-6
330
RP30-2
330
R46
R4
R45
R2
R48
R17
R47
R12
R25
R20
R36
R35
C13
20pf
C5
20pf
C35
20pf
C28
20pf
C44
50pf
C36
50pf
C56
50pf
C50
50pf
C4
50pf
CW
CCW
10125
10195
10231
10101
RP9-8
RP9-7
RP9-6
RP9-3
51
RP9-4
RP9-2
"R"
RECORD
"C"
CLOCK
FROM REC CONTROL PWB
R8
R7
R6
75
49
R11
R10
Q3
Q1
Q4
Q2
BFR-91 (2)
BFR-91 (2)
DC1
DC3
AC3
AC1
AC4
AC2
DC4
DC2

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE



1. 7L, 9H & 9K 10125 DEVICE TO BE MOTOROLA ONLY
2. ALL RESISTANCE VALUES ARE IN OHMS, 1/4 W 5%
3. 9B. 10231 DEVICE TO BE MOTOROLA ONLY

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

ENG SERV	DATE
	1/4/78

PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
			1

DO NOT SCALE DRAWING

TOLERANCE

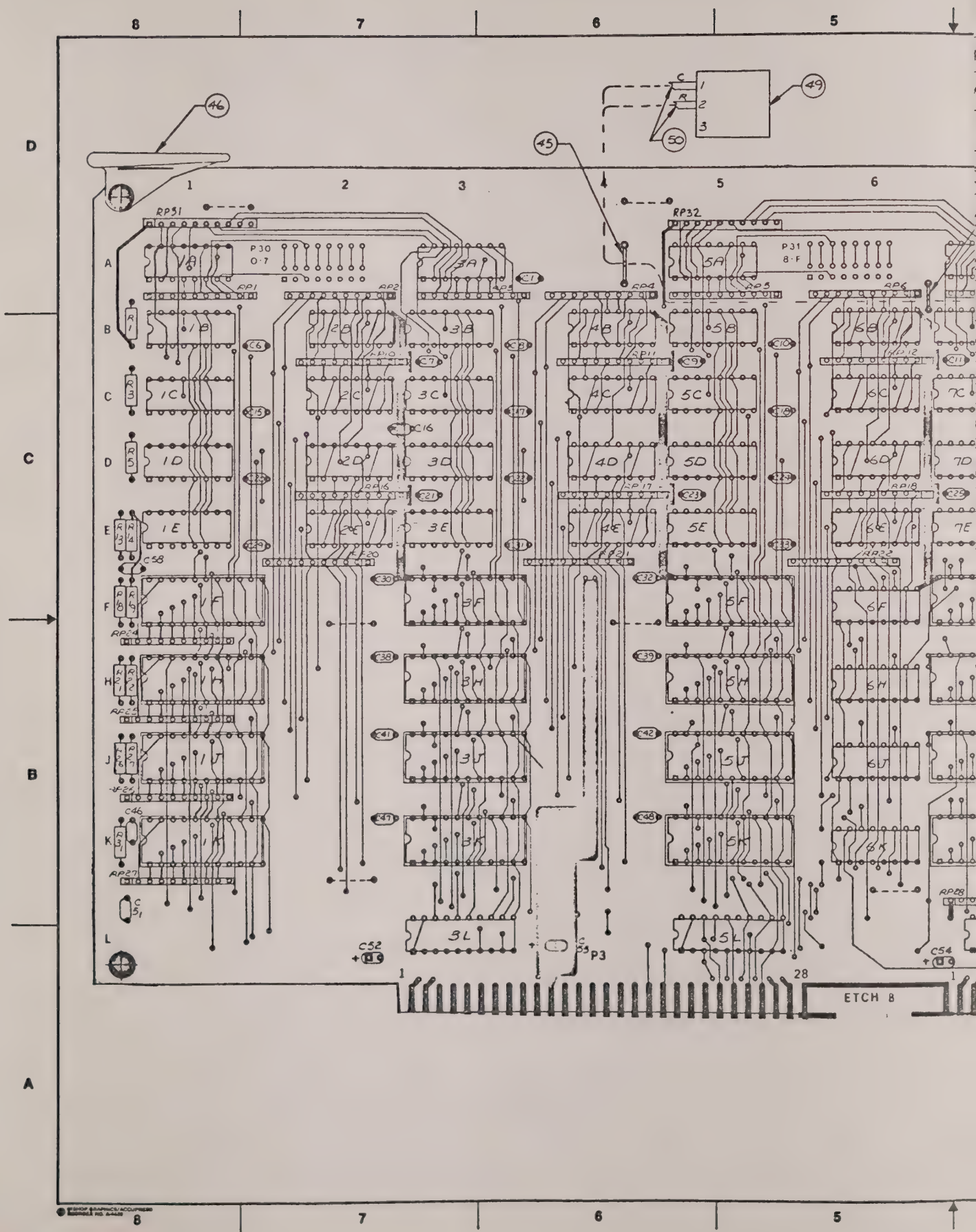
DRAWN	DATE
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR	

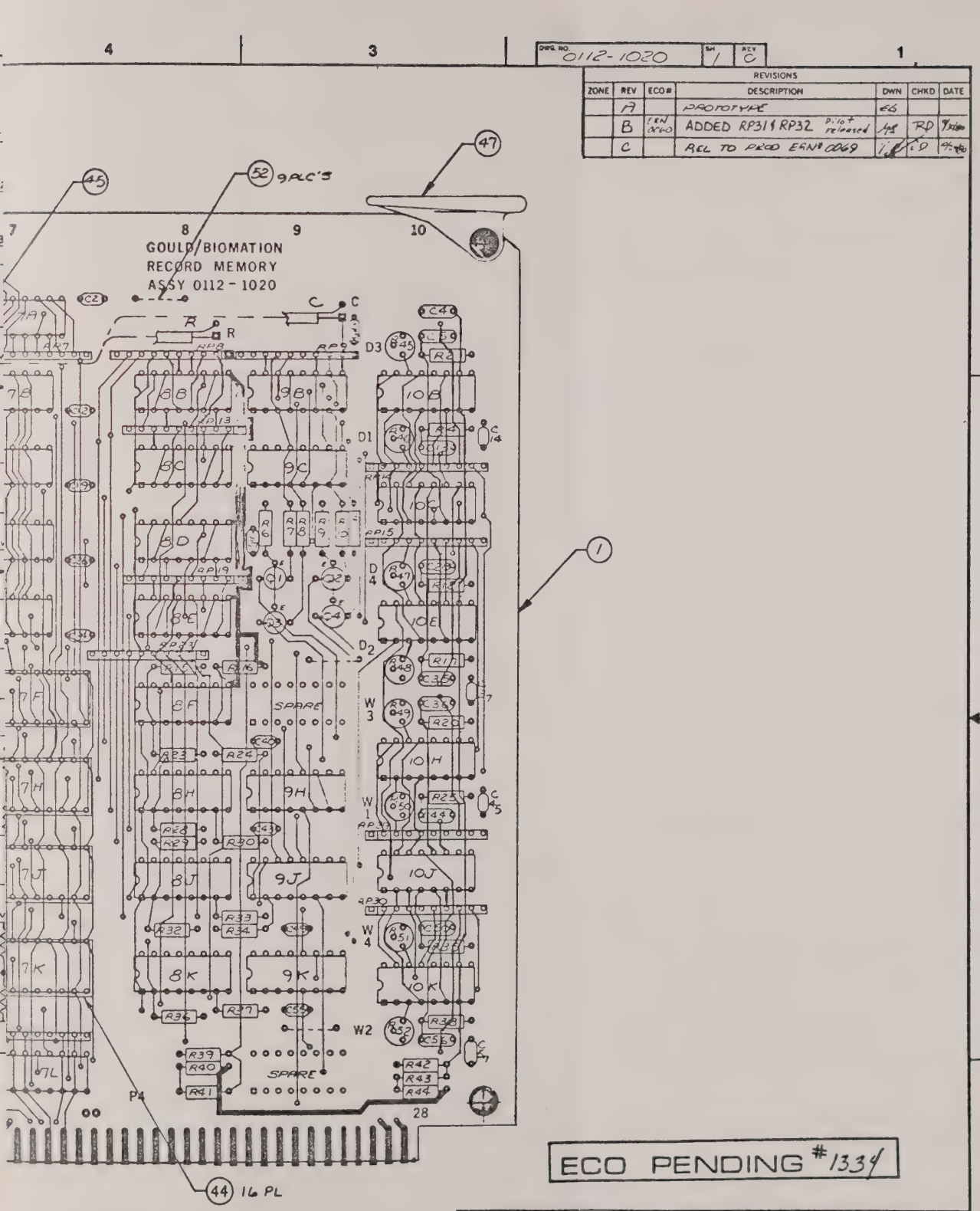
GOULD biomation

TITLE SCHEMATIC K100-D RECORD MEMORY PWB

SCALE	SIZE	PART NUMBER	REV
	D	0112-1021	C

CODE SHEET 3 OF 3


8
7
6
5
D
C
B
A
1
2
3
5
6
46
45
49
50
C
R
1
2
3
RP31
RP32
P30
0-7
P31
8-F
RP1
RP2
RP3
RP4
RP5
RP6
RP9
RP10
RP11
RP12
RP16
RP17
RP18
RP20
RP21
RP22
RP24
RP25
RP26
RP27
RP28
1A
2A
3A
4A
5A
6A
7A
1B
2B
3B
4B
5B
6B
7B
1C
2C
3C
4C
5C
6C
7C
1D
2D
3D
4D
5D
6D
7D
1E
2E
3E
4E
5E
6E
7E
1F
2F
3F
4F
5F
6F
7F
1H
2H
3H
4H
5H
6H
7H
1J
2J
3J
4J
5J
6J
7J
1K
2K
3K
4K
5K
6K
7K
1L
2L
3L
4L
5L
6L
7L
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C29
C30
C31
C32
C33
C37
C38
C39
C41
C42
C47
C48
C46
C51
C52
C53
C54
C58
P3
1
28
ETCH B


DWG NO. 0112-1020
SH 1
REV C
REVISIONS
ZONE | REV | ECO# | DESCRIPTION | DWN | CHKD | DATE
A | PROTOTYPE | EG
B | ADDED RP31 & RP32 Pilot released | RD
C | REL TO PROD ECN# 0069 | RD
GOULD/BIOMATION
RECORD MEMORY
ASSY 0112-1020
52 9AC'S
47
45
1
44 16 PL
SPARE
SPARE
P4
28
ECO PENDING #1334
PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITEM
DO NOT SCALE DRAWING
TOLERANCE
DRAWN
CHECKED
PROJ ENG
MANUFACTURING
QUALITY ASSUR
DATE
GOULD biomation
TITLE
ASSEMBLY
RECORD MEMORY P.C.B.
SCALE
SIZE D
PART NUMBER 0112-1020
REV C
CODE
SHEET OF
DASH NO. | NUMBER | QTY
NEXT ASSEMBLY
ENG SERV

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						
	-60	-50	-40	-30	-20	-10	
1						1	011
2							
3						1	185
4						4	185
5						19	185
6						—	
7						16	185
8						4	185
9						2	185
10						8	185
11						1	180
12						2	180
13							
14						16	180
15							
16						4	130
17						1	185
18							

ECO PENDING

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN E. G
CHECKED R.
ENGINEER
MANUFACTUR
QUALITY ASSU

PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
2-1022	RECORD MEMORY			P.C. BOARD	
50-0037	INTEGRATED CIRCUIT	9C	10101		
50-0059		1A, 3A, 5A, 7A	10115		
50-0074		2B,2C,2D,2E,4B,4C,4D,4E 6B,6C,6D,6E,8B,8C,8D,8E	10125	MOTOROLA ONLY	
		7L,9H,9K			
50-0061		1B,1C,1D,1E,3B,3C,3D,3E 5B,5C,5D,5E,7B,7C,7D,7E	10137	ALT. 10136 1850-0083	
0-0019		10B,10E,10H,10K	10231		
50-0048		10C, 10J	10195		
00-0208		6F,6H,6J,6K, 8F,8H,8J,8K	74S161		
00-0193		9J	74LS138		
00-0240		3L, 5L	74LS244		
20-0318	INTEGRATED CIRCUIT	1F,3F,5F,7F,1H,3H,5H,7H, 1J,3J,5J,7J,1K,3K,5K,7K	93422		
0-0038	TRANSISTOR	Q1,2,3,4	BFR-91		
0-0075	INTEGRATED CIRCUIT	9B	10231	MOTOROLA ONLY	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD
	A	PROTOTYPE				
	B	ADDED RP31 & RP32	9-26-80	MR	RD	
	B	PILOT REL ERN 0060				
#1334	C	REL TO PROD ERN # 0069				

	DATE
DD	5/27/80
Dan	10/24/80
L	9/30/80
KG	11/14/80
RANCE	11/14/80

LIST OF MATERIAL

RECORD MEMORY

biomation

B	0112-1020	REV C

MODEL K100D | CODE | SHEET 1 OF 3

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						
	-60	-50	-40	-30	-20	-10	
19						8	3
20						8	3
21						2	3
22						4	3
23						4	3
24						10	3
25						4	3
26						4	3
27							
28						8	3
29							
30							
31						15	3
32						13	3
33						4	3
34							
35							
36							

			DRAWN
			CHECKED
			ENGINEER
			MANUFACTU
			QUALITY AS
DASH NO.	NUMBER	QTY	
	NEXT ASSEMBLY		

PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
000-5106	RESISTOR	R1,3,5,7,8,10,11,13		51Ω, 1/4W, 5%	
000-3006		R2,4,12,17,20,25,35,38		30Ω, 1/4W, 5%	
000-7506		R6,9		75Ω, 1/4W, 5%	
000-2200		R23,24,32,34		220Ω, 1/4W, 5%	
000-3300		R40,41,43,44		330Ω, 1/4W, 5%	
000-4700		R14,16,19,22,27,30,33,37,39,42		470Ω, 1/4W, 5%	
000-1600	RESISTOR	R15,28,29,36		160Ω, 1/4W, 5%	
000-1200	RESISTOR	R18,21,26,31		120Ω, 1/4W, 5%	
300-0048	POT	R45,46,47,48,49,50,51,52		2K, 1TURN	
000-0060	RES. PACK	RP1,3,5,7,9,10,11,12,13,16,17,18,19,31,32		51Ω, 10PIN	
000-0035	RES. PACK	RP2,4,6,8,20,21,22,23,24,25,26,27,28		220Ω, 10PIN	
000-0034	RES. PACK	RP14,15,29,30		330Ω, 10PIN	

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE
RING	
URANCE	

LIST OF MATERIAL

RECORD MEMORY

biomation

B | 0112-1020 | REV C

MODEL K100 D | CODE | SHEET 2 OF 3

COMMENTS		TOTAL COST	UNIT COST

ASSEMBLY TIME	COMPONENT LEAD SPACING

ITEM	QUANTITY PER ASSEMBLY						
	-60	-50	-40	-30	-20	-10	
37						46	4
38						—	
39						3	4
40						4	4
41						5	4
42							
43						2	6
44						16	6
45						—	
46						1	7
47						1	01
48						2	7
49						1	6
50						2	9
51							
52						9	9
53							
54							

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN
CHECKED
ENGINEER
MANUFACTU
QUALITY AS

PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
000-0025	CAPACITOR	C1,2,3,6-12,14-27, 29-34,37-43,45-49, C51,55,57,58		.1uf, 50V	
300-0025	CAPACITOR	C52, 53, 54		47uf, 6V	
100-0006	CAPACITOR	C5,13,28,35		20pf, 5%	
100-0019	CAPACITOR	C4, 36. 44,50,56		50pf, 5%	
100-0120	SOCKET	P30, 31		16PIN	
100-0136	SOCKET	X1F, X3F, X5F, X7F, X1H, X3H, X5H, X7H, X1J, X3J, X5J X7J, X1K, X3K, X5K, X7K		22 PIN	
000-0120	EJECTOR				
12-0228-02	EJECTOR	A2		STAMPED	
200-0025	MOUSETAIL				
000-0242	CONN.			3 POS.	
000-0037-11	COAX. CABLE	C, R		11" LONG PIN	
000-0054	BUS WIRE				

REF. DRAWINGS	REV	DESCRIPTION	DATE	DWN	CKD	APPD

	DATE
RING	
SURANCE	

LIST OF MATERIAL

RECORD MEMORY

biomation

B	0112-1020	REV C

MODEL K100 D | CODE | SHEET 3 OF 3

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